CLAIMS

What is claimed is:

1. A system having a partitioned memory, said system comprising:

a processor;

a hardware implemented memory router coupled to said processor;

memory coupled to said memory router;

said memory router configured to store memory partition information, said information describing the memory allocated to said processor; and

said memory router operable to map a memory access request having an address from said processor to an address in said memory allocated to said processor.

2. The system of Claim 1, further comprising:

at least a second processor coupled to said memory router, wherein said system comprises a plurality of processors;

said memory partition information stored in said memory router further describes the memory allocated to each of said plurality of processors; and

said memory router is further operable to map memory access requests from said plurality of processors to respective addresses in said memory allocated to each of said plurality of processors.

3. The system of Claim 2, wherein:

said memory partition information further describes the type of access each processor of said plurality has to each portion of its allocated memory; and

said memory router is further operable to determine whether a memory access request having a first address from a first processor of said plurality is valid for said first address, based on the type of access and said first address.

4. The system of Claim 3, wherein said type of access is selected from the group consisting of read only, write only, and read/write access.

5. The system of Claim 2, wherein said router is re-configurable by altering said memory partition information, wherein said memory allocated to said plurality of processors is re-allocable.

6. The system of Claim 2, wherein said router is re-configurable by altering said memory partition information, wherein said type of access allocated to at least one processor of said plurality of processors is modifiable.

7. The system of Claim 2, wherein said memory router comprises a first component and a second component, said first and said second components coupled by a communication link;

said first component operable to add a key to said memory access request, said key identifying said second processor; and

said second component operable to use said key to route said request to said address in said memory allocated to said second processor, wherein multiple processors using the same communication link and using overlapping addresses securely access said memory.

8. The system of Claim 2, wherein said memory partition information is stored in a table containing a translation from processor address space to memory.

9. The system of Claim 8, wherein said table further comprises information allocating to a first processor of said plurality read only access to a first memory partition and to a second processor read and write access to said first memory partition.

10. The system of Claim 2, wherein more than one processor has access to a memory partition, wherein said memory is shared and said memory router has control over memory access.

11. The system of Claim 2, wherein said plurality of processors are coupled to said memory router via a single communication link.

12. The system of Claim 2, wherein said plurality of processors are coupled to said memory router via a plurality of communication links.

13. The system of Claim 2, wherein a first processor of said plurality runs a first operating system and said second processor of said plurality runs a second operating system and wherein said second processor is allowed to read the memory allocated to said first processor but is not allowed to write to said memory allocated to said first processor.

14. A method of partitioning memory, said method comprising the steps of:

a) a hardware implemented memory router receiving a request for memory access from one of a plurality of processors, said request specifying a first address;

b) said hardware memory router determining the location in memory corresponding to said first address, said memory partitioned among said plurality of processors; and

c) said hardware memory router routing said memory request to said memory, wherein said memory access is securely executed such that said one of said plurality of processors is only able to access memory which is allocated to it.

15. A method of partitioning memory as recited in Claim 14 further comprising the step of:

d) re-partitioning said memory by re-configuring said hardware memory router.

16. A method of partitioning memory as recited in Claim 15 wherein said step d) comprises the step of:

d1) re-configuring said memory router with commands entered via an external port to said memory router, wherein software executing on said plurality of processors is unable to modify said memory router.

17. A method of partitioning memory as recited in Claim 14 further comprising the step of:

d) changing the type of access that said one processor of said plurality has to a portion of said memory by re-configuring said memory router.

18. A method of partitioning memory as recited in Claim 17 wherein said type of access is selected from the group consisting of read only, write only, and read/write access.

19. A method of partitioning memory as recited in Claim 17 wherein said step d) further comprises the step of:

d1) periodically re-configuring said memory router.

20. A method of partitioning memory as recited in Claim 14 further comprising the steps of:

d) adding information to said memory request, said information specifying the processor of said plurality of processors which made said memory request, said plurality of processors sharing a communication link; and

e) after receiving said memory request via said communication link, said memory router using said information to determine which processor made said memory request.

21. A hardware implemented memory router comprising:

an input to receive an memory access request, said request specifying an address in a first processor's of a plurality of processors address space;

a table for storing memory partition information, said information describing the memory allocated to each of said plurality of processors; and

logic operable to translate said address in said processor address space to a corresponding address in said memory.

22. The hardware implemented memory router of Claim 21, wherein:

said memory partition information further describes the type of access each processor of said plurality has to each portion of its allocated memory; and

said memory router is further operable to determine whether said memory request from said first processor is valid for said address specified in said request, based on the type of access and said address specified in said request.

23. The hardware implemented memory router of Claim 21, wherein said memory router comprises a first component and a second component, said first and said second components coupled by a communication link;

said first component operable to add a key to said address specified by said processor request, said key identifying the processor of said plurality making said request; and

said second component operable to use said key to route said request to the appropriate memory address, wherein multiple processors using the same communication link and using overlapping processor addresses securely access said memory.